



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,066	08/29/2003	Tim Murphy	501039.04	9772

7590 04/29/2005

Steven H. Arterberry, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

EXAMINER

IM, JUNGHWA M

ART UNIT PAPER NUMBER

2811

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No. 10/652,066	Applicant(s) MURPHY ET AL.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 50-54 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 50-54 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 8, 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 50, 51, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nhu (US 5237441) in view of Sudo (US 5198684).

Regarding claim 50, insofar as understood, Fig. 2 of Nhu shows a computer system, comprising:

- a data input device (connected to an input terminal 16);
- a data output device (connected to an output terminal 18);
- a processor (80, 82) coupled to the data input and output devices; and memory device (42) including a chip package (20 in Fig. 4) having a plurality of conductors (24, 26 in Fig. 4) coupled to the processor, the memory device the memory device including,

Art Unit: 2811

a chip (10, 42) including memory circuitry, the memory circuitry including,
an address decoder (100) coupled to an address bus;
a read/write circuit (94, 96, 98) coupled to a data bus;
a control circuit (92) coupled to a control bus;
a memory-cell array (90) coupled to the address decoder, control circuit, and
read/write circuit, the memory-cell array; and
a chip package (20) physically coupled to the chip.

Nhu shows most aspects of the instant invention except that a first convert in the memory circuit to convert the corresponding EM signals to electric signals (and visa versa) and a second convert in the chip package to receive the converted signals from the first converter converting back.

Fig. 1 of Sudo shows a light transmit-receiving elements (40A, 40B) with two converters (42B, 44B) formed on chip package (10). And Sudo further discloses that the first converter (44B) is operable to convert the electric signal to an optical signal (EM signal) and visa versa and the converted signals coupled to the second converter (42B) while the second converter converting the EM signal to an electrical signal to the IC circuit on the package substrate (col. 6, lines 33-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Sudo into the device of Nhu in order to have "a first converter coupled to the address, data, and control busses, the first converter operable to data signals on the data bus and convert the data signals into corresponding data output electromagnetic waves, and operable to receive address, data, and control electromagnetic waves

Art Unit: 2811

and convert these electromagnetic waves into corresponding electric address, data, and control signals that are applied on the address, data, and control busses, respectively; and a chip package physically coupled to the chip, the chip package including a second converter that is operable to receive the data output electromagnetic waves from the first converter and convert these received electromagnetic waves into corresponding electric data output signals that are applied to corresponding conductors, and the second converter operable to receive electric address, data, and control signals on corresponding conductors and to convert these electric signals into corresponding address, data, and control electromagnetic waves that are communicated to the first converter” since such a configuration improves a integration density of the IC. See col. 1, lines 22-30 of Nhu’s specification.

Regarding claim 51, Nhu discloses the electromagnetic waves comprise optical electromagnetic signals (col. 1, lines 38-40).

Regarding claim 53, Sudo discloses the first and second converters comprise laser diodes (col. 6, lines 54-59).

Regarding claim 54, the combined teachings of Nhu and Sudo fail to disclose that “the memory device comprises a dynamic random access memory.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a DRAM for the memory device of Nhu and Sudo since DRAM memory chips consume less power than other kind of memory chips.

Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nhu and Sudo as applied to claim 1 above, and further in view of Austin et al. (US 5200631), herein after Austin.

Claim 52, the combined teachings of Nhu and Sudo shows the most aspect of the instant invention except “the electromagnetic waves comprise infrared electromagnetic waves.” Austin discloses a semiconductor package wherein the electromagnetic waves comprise infrared electromagnetic waves (col. 4, line 68 - col. 5, line 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a infrared EM wave application to the device of Nhu and Sudo with the teachings of Austin to broaden the range of the device application.

Response to Arguments

Applicant's arguments filed March 8, 2005 have been fully considered but they are not persuasive. Below are Examiner's remarks in response to Applicant's arguments.

Applicant mainly argues, “The Nhu reference does not disclose or fairly suggest that the circuit board 20 includes a converter that is operable to receive the data output electromagnetic waves from another converter and convert these received electromagnetic waves into corresponding electric data output signals that are applied to corresponding conductors, and the converter operable to receive electric address, data, and control signals on corresponding conductors and to convert these electric signals into corresponding address, data, and control electromagnetic waves that are communicated to the converter,” and “The Sudo reference does not disclose or fairly suggest effecting communication between the semiconductor chips 30 and the underlying silicon substrate 20 by converting electromagnetic signals to electric signals.” First, the Nhu reference is introduced to show an IC built on the chip package except the signal converters between the chip and the package. And the Sudo reference is further referred to

Art Unit: 2811

compliment the deficiency of the Nhu reference. That is, a converter between the chip and the package. As discussed in detail in the Office action, Sudo discloses that the first converter (44B) converts the electric signal by the chip to an optical signal (EM signal) outputting to the substrate of the package substrate through coupling to the second converter which converts received EM signal into the electrical signal. See Abstract and a portion of column 6, lines 33-65. Second, it appears that the Applicant implies that a limitation of having data, address and control signals is patentably distinct. However, input/output signals of data, address and control are essential/inherent elements in data/information process in an IC. That is, a signal/data is received through the data line while carried by the address line with incorporation of the control circuits as shown in Fig. 2 of Nhu.

Applicant further argues, "Neither the Sudo nor Nhu reference provide any motivation or suggestion to modify the disclosure of the Sudo reference so that the semiconductor chips 30 attached to the substrate 20 communicate with each other by converting an electromagnetic signal to an electric signal or vice versa." The Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 595 (CCPA 1969).

3. The rejection under 35 U.S.C. 112, second paragraph is withdrawn.

Art Unit: 2811

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800